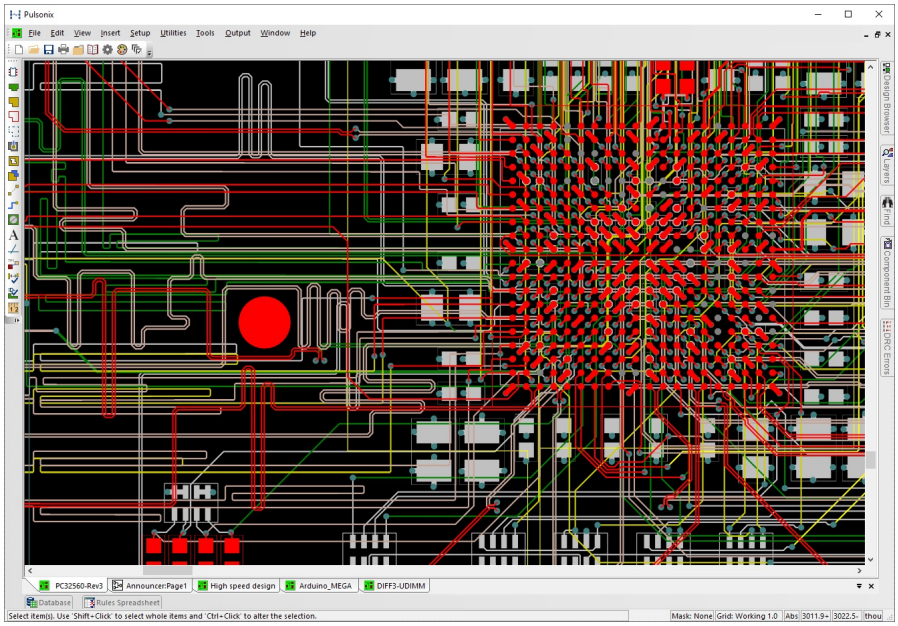
Pulsonix Version 11.0 Update

New Graphics Engine

Significant speed improvements have been made to Pulsonix by completely rewriting the underlying graphics engine to utilise the standard DirectX graphics. This standard means high performance graphics cards such as those used in the gaming industry with powerful GPU chip sets can used and taken advantage of. As well as the speed advantage, the new graphics also improves the rendering quality of the design image being viewed in Pulsonix. Speed increases of up to 80% on large designs have already been seen with customers.

The introduction of auto-pan means super-smooth panning in the Schematics Editor with Version 11.



Extensive Multi-threading Technology

Multi-threading capability has been extended and added to many functions in Pulsonix, such as Design Rules Checking (DRC), Copper Pouring and Net Optimisation to name a few. With processor multi-core capabilities, it means that speed within Pulsonix can be significantly increased on features that are processor intensive and can utilise parallel processing.

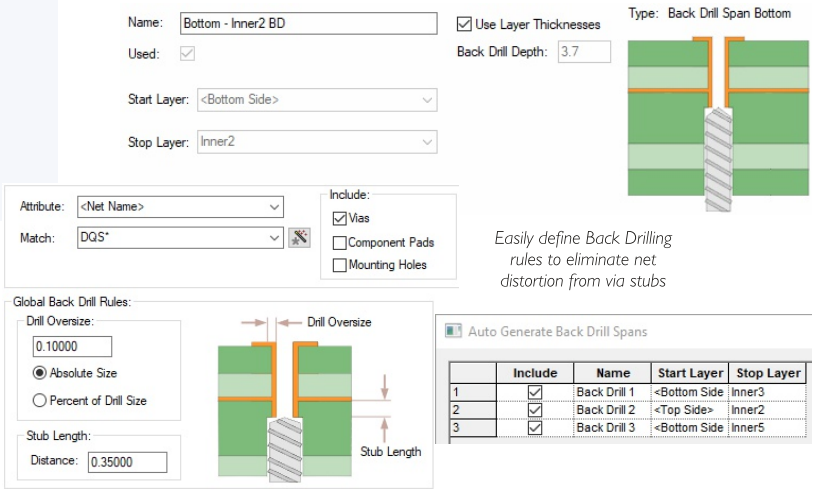
Multi-threading improvements are shown for in options utilising this technology and 8 Cores:	Average Speed Improvement
Design Rules Checking (DRC)	65%+
CAM Plot of Gerber file generation	65%
Rules Spreadsheet Bar for High-Speed designs	60%+
Copper pouring of copper template shapes	75%
Clear All Copper Pour Templates	60%
Net Optimisation on large nets	60%

Extended Character Set (Unicode)

Extended character and internationalisation support using the Unicode standard has been added to Pulsonix. As well as character sets for languages such as Chinese and Korean, Pulsonix 11 will also support technical characters such as Ω, ≠, ≤, ≥, ±

Back Drilling for High-Speed Designs

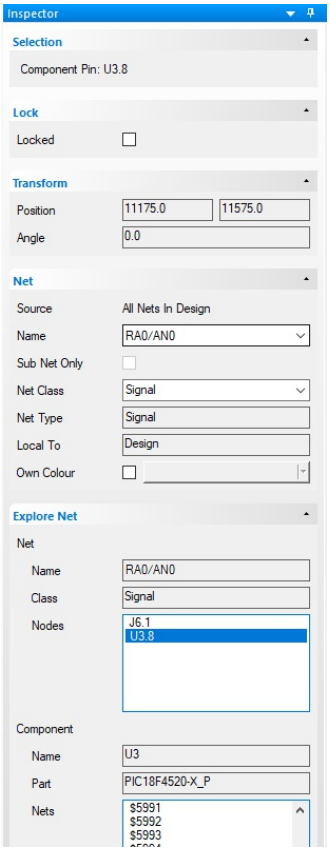
Pulsonix 11 introduces new functionality to its High-Speed design option to enable Back Drilling. Using an easily created rule set, Back Drilling can be defined for nets that require the removal of unwanted via or component pin stubs on through-holes. This can significantly remove signal integrity issues and signal distortion. Stubs are created when a via has unused portions of its layer stack to the outer layers of the board. With the rule sets defined, Back Drilled vias in the design can be quickly identified and located. Specific NC drilling outputs can be created for Back Drilled vias based on their rules.



Easily define Back Drilling rules to eliminate net distortion from via stubs

Dynamic Properties (Inspector) Bar

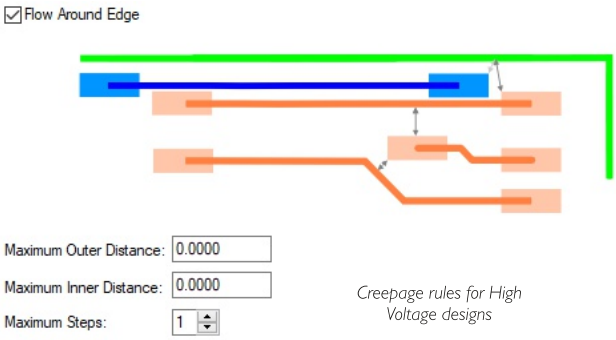
The new Inspector Bar brings dynamic object properties to the Pulsonix work space. This interactive dockable bar can be displayed at all times presenting specific information on selected design content in real time as you need it. Design items are grouped into logical functional blocks in the panel and can be customised to prioritise information that is important to you.



Properties for objects selected in your design are displayed dynamically in the new Inspector Bar

Creepage Rules definition and checks

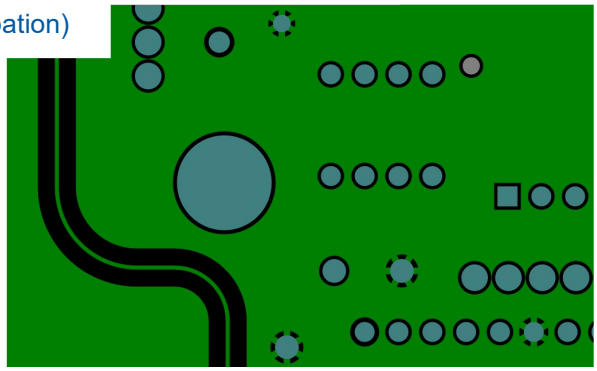
The new Creepage rule in Pulsonix 11 allows you to identify critical nets and define rules for them. Typically, these would be nets within high voltage designs. This rule differs from standard spacing rules in that this defines the shortest path between two conductive entities but can be measured across surfaces, through air gaps and around the edge of the board.



Creepage rules for High Voltage designs

Copper Neck Width Rules (Power Dissipation)

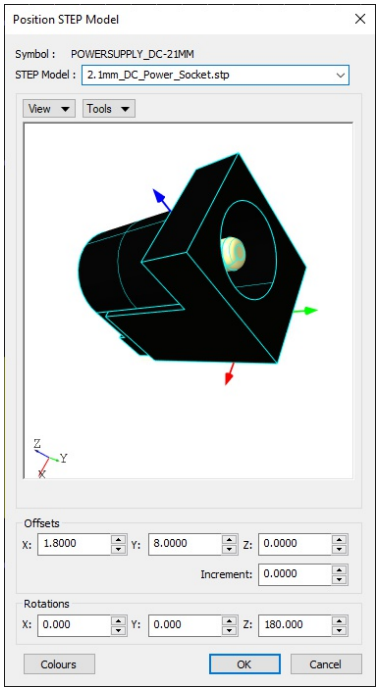
New Copper Neck Width rules in Pulsonix 11 enables plane areas where 'pinching' of copper between two pads to be defined and then checked. Typically, where power planes are used for power dissipation, pinching is undesirable and should be eliminated. Using a minimum neck width rule on nominated nets, more normalised pad and via distribution can be obtained.



Reduce power dissipation issue using the new Copper Neck Width rule

STEP Improvements

Improvements have been made to the STEP interface including a significant speed increase by using background STEP file creation that is automatically updated as the design changes. Footprint to STEP model alignment has been improved and now includes tools for model orientation and alignment. For STEP import into the PCB design, Mounting Holes and Vias from STEP models can be imported, further enhancing the capabilities and visualisation of your design. In addition, Board Placement Sites can be imported to aid component placement of critical devices.

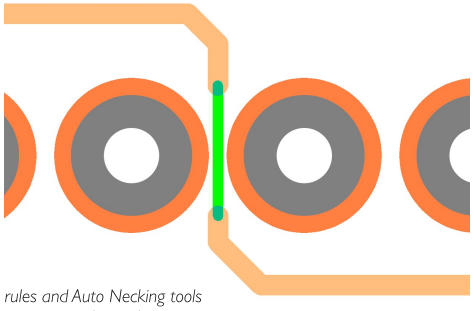


STEP improvements in Pulsonix 11 further enhances the Pulsonix 3D PCB experience

Auto Necking from SM Pads

New Pad Auto Necking rules enable stub rules to be obeyed when the track thickness is determined to be too 'fat' for the surface mounted pad it exits from. By defining a percentage of track to pad ratio and a minimum stub length, during routing these rules can be automatically enabled and used without further manual intervention.

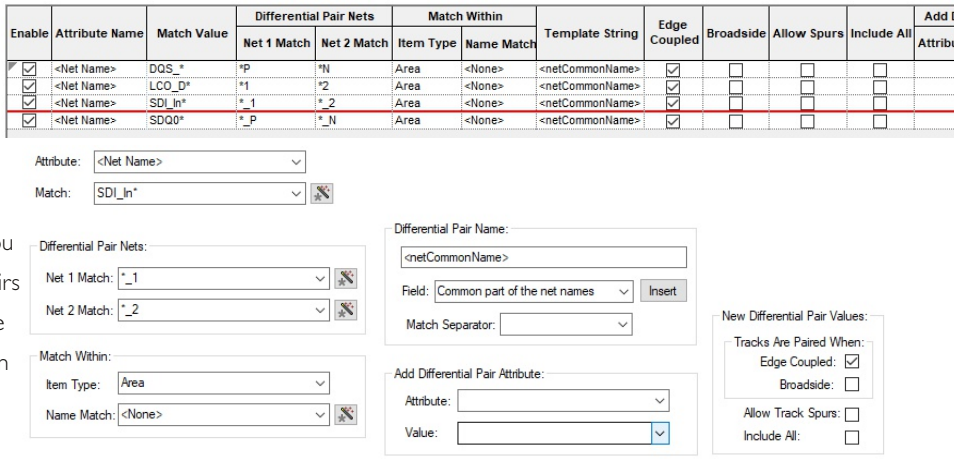
The additional Auto Necking tool enables the alternative track style to be utilised when necking down. This would provide the clearance required to route a track through a 'gap', between two pads for example.



New Auto Pad Necking rules and Auto Necking tools provide faster editing options on dense designs

Differential Pair Rules & Improvements

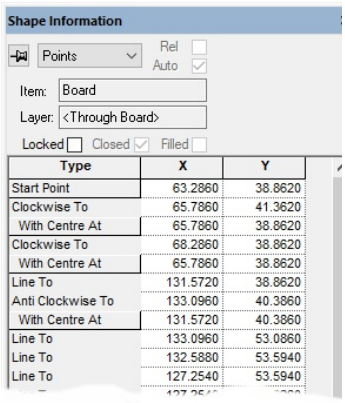
Create Differential Pair rules using the new rules definitions within the Technology. Flexible rules are easily defined using net attributes and wildcarding which can be as unique or general depending on preference. When specific Differential Pair via patterns are created, such as with ground return, you can now copy this pattern and reuse it on other Pairs in the design. Additional features to further enhance routing with Pairs includes, auto-turn direction when changing layers and creating a via pattern and the display of a legal completion path shown when routing the Pair.



Differential Pair rules enable the automatic creation of multiple Pairs with ease

Shape Information/Editing Bar

With the new sliding shape Information Bar, any shape can be created and edited in a grid style pane. Editing shapes can be modified using selected commands and modes, ranging from lengths to points, and absolute or relative coordinates. All shapes, includes lines, arcs and radius can be edited by simply selecting the shape. Where more complex shapes are edited, the dialog can also be used to find and highlight the segment required.



Edit shapes in the design using the graphical Shape Information Bar

Import IPC-2581 Layer Stackup

To further support complex layer structures, files created in IPC-2581 format can be imported into the Layers dialog from external sources where the layer stack has been calculated. This enables a full layer stack with impedance considerations to be generated externally and imported into Pulsonix easily.

Name	Associated Layer	Class	Side	Bias	Net	Material	Thickness
	Assembly Top	Assembly	Top	None			0.000
	Silkscreen Top	Silkscreen	Top	None			0.000
	Paste Mask Top	Paste Mask	Top	None			0.000
	Solder Mask Top	Solder Mask	Top	None		Mask (0.025)	0.025
Top		Electrical	Top	None		Copper Foil	0.036
Prepreg A		Construction		None		Prepreg (0.11)	0.110
Prepreg B		Construction		None		Prepreg (0.11)	0.110
DIELECTRIC_1		Prepreg	Inner	None		PrePreg 3113	0.060+
Ground		Electrical	Inner	None		FR4 Core Cu	0.053
Substrate		Construction		None		FR4 (1.0)	1.000
DIELECTRIC_2		Core	Inner	None		FR4 Core	0.075
Power		Electrical	Inner	X		Copper 1oz (0.035)	0.035
Prepreg D		Construction		None		Prepreg (0.11)	0.110
Prepreg C		Construction		None		Prepreg (0.11)	0.110
DIELECTRIC_3		Prepreg	Inner	None		PrePreg 1080	0.069
DIELECTRIC_4		Prepreg	Inner	None		PrePreg 7628	0.184
DIELECTRIC_5		Prepreg	Inner	None		PrePreg 1080	0.069
L4		Electrical	Inner	None		FR4 Core Cu	0.035
DIELECTRIC_6		Core	Inner	None		FR4 Core	0.300
L5		Electrical	Inner	None		FR4 Core Cu	0.035
DIELECTRIC_7		Prepreg	Inner	None		PrePreg 1080	0.069
DIELECTRIC_8		Prepreg	Inner	None		PrePreg 7628	0.184
DIELECTRIC_9		Prepreg	Inner	None		PrePreg 1080	0.069
L6		Plane	Inner	None		FR4 Core Cu	0.035
DIELECTRIC_10		Core	Inner	None		FR4 Core	0.075
L7		Electrical	Inner	None		FR4 Core Cu	0.053
DIELECTRIC_11		Prepreg	Inner	None		PrePreg 3113	0.060+
Bottom		Electrical	Bottom	None		Copper Foil	0.036
	Solder Mask Bottom	Solder Mask	Bottom	None		Mask (0.025)	0.025
	Paste Mask Bottom	Paste Mask	Bottom	None			0.000

Create complex layer stacks using the new tools and import mechanisms available

To further aid speed of creating complex layers, the Layers dialog now also allows a full Export and Import of CSV files. Another new feature when manually creating layer stacks is the Reflect Layer Stack feature which enables 'half' of the stack to be defined and then auto-completed as a mirror image using the Reflect button.

Feature Summary:

- User Defined Pad Shape Improvements
- Vertical Text Alignment for Multi-line Text
- Track & Vias styles in SCM Translated to PCB
- Weld multiple Components to a Bus segment
- New PCB Wizard
- Auto-Pan feature
- Optimise Settings for Large Nets
- Large Net Warning on Optimise All Nets
- Dynamic Align of items
- Select from popup list
- Dynamic Attributes for Part Editor Description field
- Override Readable Orientation of Text
- No Connect Pin Highlight Colour
- New Signal Reference Type - Net labels
- Mounting Hole Symbols in Schematic
- Micro-Via to Buried Via Stagger Spacing
- New Design Rule Manufacturing Checks
- Enhanced Dimensioning features
- New Line Select Mode
- Select Track Paths by selecting Components
- Scaling design items; Shapes, Symbols, Text, Bitmaps
- Export to ZIP format through Plotting dialog
- Plotting output to SVG Device
- Track Impedance Calculator
- Chip-On-Board Option interaction improvements
- Ability to load partial Colour files

Pulsonix

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